Each PMOS transistor in Fig. 2 is located in an isolated n-well to minimise the threshold voltage mismatch caused by the body effect. An ordinary current mirror circuit (M5 and M6) generates $I_o$, such that:

$$I_o = \frac{b_3(V_{DD} - 3V_{TH})^2}{2(1 + 2\sqrt{m_2})^2}$$

(3)

where $m_3 = \beta_3\beta_4$, and $I_o$ is assumed.

Since the voltage drop across the resistor $R$ is equal to the potential difference between the source nodes of M16 and M18, $I_o$ can be derived as follows by using the strong inversion current equation:

$$I_o = \frac{2(1 - \sqrt{m_3})^2}{R\beta_8}$$

(4)

where $m_1 = \beta_3\beta_4$, and $\beta_8 = \beta_3$. The current component $I_1$ and $I_2$ can be obtained easily from $I_o$ and $I_1$, by multiplying the transistor size ratios of the cascaded current mirror circuit (M9-M12) and the simple current mirror circuit (M13-M15, M17). Hence, the final output current $I_o$ can be derived as

$$I_o = \frac{1 - \sqrt{m_5}}{1 + 2\sqrt{m_2}} \sqrt{m_1 m_4} (V_{DD} - 3V_{TH})$$

(5)

where $m_5 = \beta_3\beta_4\beta_5$ and $\beta_5 = \beta_3$. As shown in eqn. 5, the mobility dependence terms are completely cancelled out in $I_o$, if we assume that the mobility of the same type devices (NMOS, PMOS) is the same for all the transistors in the circuit. The temperature dependence on the left in the $I_o$ expression of the eqn. 5 comes from the temperature dependences of $V_{TH}$ and $R$. The temperature dependences of these two parameters tend to cancel each other since the diffusion resistor $R$ and the PMOS threshold voltage $V_{TH}$ have positive and negative temperature coefficients, respectively. Fig. 3 shows the average output current values of 12 samples, with a 1.7% variation for a temperature range of 0 to 75°C.

© IEE 1996

Electronics Letters Online No: 19960827

C.-H. Lee and H.-J. Park (Department of Electrical Engineering, Pohang University of Science and Technology/PILR, Sun 31 Hyojong-dong, Pohang, Kyungbuk, 790-784, Korea)

References

Kernel based precomputation scheme for the design of low power combinational circuits

L.-S. Choi, H. Kim, D.-W. Seo and S.-Y. Hwang

Indexing terms: VLSI, Combinational circuits

The authors present a synthesis algorithm for designing low power combinational circuits by eliminating unnecessary signal transitions. Transforming a given circuit by selecting a kernel as a precomputation logic, the proposed algorithm reduces power dissipation by disabling a portion of the circuits. Experimental results show that the algorithm is efficient for designing low power combinational circuits.

Fig. 1 Various precomputation architectures for low power

- a) Combinational circuit
- b) Architecture based on precomputation scheme
- c) Architecture based on Shannon expansion
- d) Proposed kernel-based precomputation architecture

Kernel based precomputation scheme: Fig. 1 shows the various schemes employed for low power design of combinational circuits. For the combinational circuit of Fig. 1a, Fig. 1b and c depict the
circuits based on a precomputation scheme and a Shannon expansion scheme, respectively. In the Shannon expansion scheme, a circuit is divided by an input variable, but a logic network can be divided more efficiently by common logic parts. We used a kernel as the common logic parts and implemented it as a precomputation logic. Fig. 1d shows the proposed precomputation architecture based on the kernel. The proposed scheme consists of three subcircuits: a precomputation logic synthesised for kernel $k$ and two subcircuits generated from the original circuit divided by the kernel $k$ and its complement $\bar{k}$. Only one subcircuit is activated while the other is disabled by setting the load-enable signal of its input register. The output of the precomputation logic is connected to the select line of a multiplexer which chooses the correct output. In Fig. 1d, $I$ is the primary input variables and $I'$ is a subset of input variables used in precomputation logic. If the mux is implemented by the transmission gate in a word-high form, only one transmission gate is added to each output line.

Fig. 2 Various schemes for low power design of combinational circuits

- Circuit-1: combination circuit
- Circuit-2: circuit transformed into precomputation scheme
- Circuit-3: circuit transformed into Shannon expansion scheme
- Circuit-4: kernel-based precomputation scheme

An example of a combinational circuit is shown in Fig. 2a, which is obtained by using script.rugged [6]. If the signal probability of inputs is 0.5, power dissipation of this circuit is 75.2uW. Fig. 2b and c shows the circuits transformed by the precomputation based scheme and the Shannon expansion scheme, respectively. The power dissipation of the precomputation based circuit is 98.5uW, while that of the Shannon expansion circuit is 58.9uW. The circuit of Fig. 2d obtained by the proposed scheme consumes 35.9uW, showing improved performance.

Logic synthesis algorithm for low power: The proposed algorithm is divided into three steps: BDD creation, kernel extraction and selection, and the circuit synthesis process. Constructing a BDD for each output, the algorithm identifies the kernels and selects the best kernel that can lead to reduction of the switching activities in the circuit. Using the selected kernel as the precomputation logic, the algorithm generates the circuit consisting of the subcircuits implementing the cofactors of the kernel and its complement. These two subcircuits are selectively enabled by the precomputed logic. The power dissipation of the kernel based scheme is obtained by eqn. (1).

$$P_{\text{net}} = P_{\text{on}} + P_i(t) \times P_{\text{on}} + (1 - P_i(t)) \times P_{\text{off}}$$ (1)

Here, $P_i(t)$ is the signal probability at the output node i of the precomputation logic. $P_{\text{on}}$, $P_{\text{off}}$, and $P_{\text{off}}$ are power dissipations at the subcircuit for $k$, $f_1$, and $f_2$, respectively.

The power estimation for a logic circuit is meaningless without a knowledge of the structure, since the power dissipation of a circuit varies according to the circuit structure. The smaller circuit does not always consume less power. However, the size of a circuit can be used as a measure of power in most cases. We use the ROBDD size as a measure of power dissipation instead of using power estimation in establishing a cost function for finding the best kernel. The cost function for selecting the best kernel for low power design is given by eqn. (2).

$$C = |k| + p(i) \times |f_1| + (1 - p(i)) \times |f_2|$$ (2)

where $|k|$, $|f_1|$, and $|f_2|$ are the sizes of ROBDDs for kernel $k$, $f_1$, and $f_2$, respectively. We select the kernel with the lowest cost.

Experimental results: The proposed algorithm has been implemented and integrated within the SIS logic synthesiser [6]. Power dissipations between the precomputation scheme and the proposed scheme for MCNC benchmark circuits are compared, and are presented in Table I. The measurements are made at a clock frequency of 20MHz using the zero-delay model. Circuit 151m cannot be synthesised using the precomputation scheme, and its power consumption is compared with the original circuit. As shown in Table I, power dissipations are reduced in most of the benchmark circuits using the proposed algorithm. The reduction of the power dissipations in the circuits generated by the proposed algorithm amounts to 57.6 and 44.8% on average, when compared with the original circuits optimised for area and those by the precomputation scheme, respectively. The resultant circuits require 13.9% less area than those using the precomputation scheme. When compared to the original circuits, the area is increased by 47.5% on average.

Conclusions: In this Letter, we have presented a new precomputation scheme and a logic synthesis algorithm for designing low power combinational circuits. The proposed algorithm transforms a given circuit by using a common kernel as the precomputation logic in a Shannon expansion scheme in order to minimise the switching activities of a circuit. The advantage of this architecture is that it can be applied to all kinds of logic functions, unlike the previous architectures which require an ODC precomputation logic. Experimental results show that the proposed algorithm is efficient for designing low power combinational circuits.

Acknowledgment: This work was supported by the Korea Science and Engineering Foundation under Grant No. 961-0919-101-2.
Enhancement of SHG efficiency in periodically poled LiNbO$_3$ waveguide utilising a resonance effect


Indexing terms: Optical harmonic generation, Lithium niobate, Optical waveguide

A resonant LiNbO$_3$ waveguide quasi-phase-matched second harmonic generation (SHG) device has been demonstrated. The resonator consisted of a channel waveguide and two dielectric mirrors attached to the waveguide facets. A normalised SHG efficiency of 400%/W and eightfold enhancement of the efficiency utilising a resonance effect were achieved.

Introduction: Efficient waveguide quasi-phase-matched second harmonic generation (QPM-SHG) devices with ferroelectric-domain-inverted gratings have been reported [1 - 5]. Although they are travelling-wave SHG devices, higher efficiency can be expected in resonant SHG devices because of power buildup of the optical waves in the resonator [6 - 8]. A resonant waveguide SHG device has been first demonstrated by Regener et al. using crystal birefringence for phase-matching [6], and preliminary experiments of resonant waveguide QPM-SHG devices have been performed [7, 8]. We propose a resonant waveguide QPM-SHG device and demonstrate eightfold enhancement of SHG efficiency by utilising a resonance effect.

Device description: Fig. 1 illustrates the resonant LiNbO$_3$ waveguide QPM-SHG device. The waveguide cavity consists of an annealed/proton-exchanged (APE) channel waveguide and two dielectric mirrors attached to the polished end facets of the channel waveguide. The mirrors have high reflectivity for the pump wave, but are almost transparent for the SH wave. Hence, only the pump wave can resonate. An electro-optic phase modulator is fabricated to tune for pump resonance. A ferroelectric-domain-inverted grating is fabricated to accomplish QPM at the pump wavelength. In this device configuration, the input pump wave can satisfy both the resonant condition and the QPM condition, and high power SH output can be obtained.

Design and fabrication: We designed a resonant waveguide QPM-SHG device for blue-light generation. The grating period was 3μm for QPM at the pump wavelength of 865nm. The grating length was 3mm. The cavity length was 7mm, and the reflectivities of the front and rear mirrors were determined to be 70 and 99%, respectively, to construct a matched resonator [6]. The length, width and gap of the electrodes of the phase modulator were 3mm, 3μm and 3μm, respectively. We estimated the device performance theoretically under no-pump-depletion approximation [6]. In the calculation we assumed a propagation loss of 1.1dB/cm, which was the value of the fabricated waveguide measured using the Fabry-Perot method [9]. The expected finesse was 9, and the expected enhancement of SHG efficiency by the resonant effect was 11.

The domain-inverted grating was fabricated in a z-cut LiNbO$_3$ crystal 0.15mm thick using a voltage pulse [1, 2]. The applied voltage was 3.5kV and the pulse duration was automatically controlled by an inversion-charge monitor [2]. Channel waveguides 3μm wide were formed by selective proton-exchange in pure benzoic acid at 205°C for 20min followed by thermal annealing at 350°C for 12h. Al electrodes for the modulator were fabricated on an SiO$_2$ buffer layer. Front and rear dielectric mirrors were attached to the waveguide end facets using ultraviolet adhesive.

Experimental results: We measured the wavelength dependence of the cavity transmittance using a DFB laser diode. A resonance curve FWHM of 4pm and finesse of 8 were obtained.

**Fig. 2 Dependence of SH output power on device temperature**

SHG experiments were performed using a laser diode of 865nm lasing wavelength. A pump wave was end-coupled through an optical isolator, a λ/2 plate and an objective, and a TM-like pump wave was excited in the waveguide cavity. Part of the pump wave was sampled into a Fabry-Perot analysers to confirm single longitudinal-mode operation of the laser diode. We measured the dependence of the SH output on the device temperature, and the results are shown in Fig. 2. The peaks of the output power show the resonance of the pump wave. The envelope of the peaks shows the temperature response curve of the QPM. The device satisfies both the resonant condition and the QPM condition at 11.7°C. Therefore we measured the SHG efficiency at 11.7°C without applying voltage to the phase modulator. Fig. 3 shows the measured efficiency against pump power. The solid line shows the result of the resonant device, and the dashed line shows that of the travelling-wave device before attaching the cavity mirrors. We achieved a normalised SHG efficiency of 400%/W, which was eight times as high as that of the travelling-wave device. The obtained enhancement factor was smaller than the theoretical value of 11. The discrepancy is probably caused by excess losses due to imperfections in the mirror alignment.